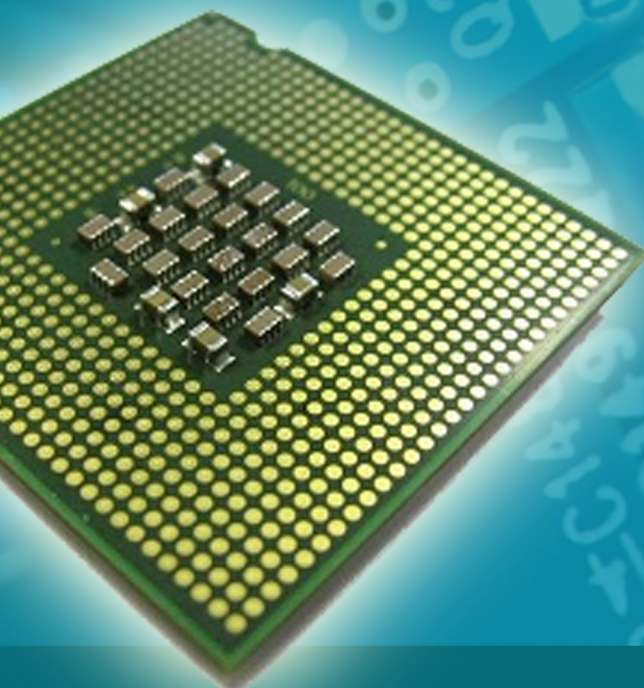




SPIRO
SOLUTIONS PVT LTD

VLSI

PROJECT TITLE
2015 - 2016



VLSI

S.NO	PROJECT CODE	TITLE	APPLICATION	YEAR
DOMAIN: AREA EFFICIENT				
1.	ITVL01	High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels	ULTRA SPEED NETWORK	2015
2.	ITVL02	An Efficient Constant Multiplier Architecture Based on Vertical-Horizontal Binary Common Sub-expression Elimination Algorithm for Reconfigurable FIR Filter Synthesis	RECONFIGURABLE FIR FILTER AND SDR SYSTEM	2015
3.	ITVL03	Trade-offs for Threshold Implementations Illustrated on AES	CRYPTOGRAPHY	2015
4.	ITVL04	A Modified Partial Product Generator for Redundant Binary	MODIFIED BOOTH	2015

		Multipliers	ENCODING AND RB PPG	
5.	ITVL05	Reviewing High-Radix Signed-Digit Adders	MULTIPLIER RECORDER	2015
6.	ITVL06	Critical-Path Analysis and Low-Complexity Implementation of the LMS Adaptive Algorithm	LEAST MEAN SQUARE ALGORITHMS	2014
DOMAIN: LOW POWER				
7.	ITVL07	Implementation of Sub threshold Adiabatic Logic for Ultralow-Power Application	ADIABATIC LOGIC AND LOW POWER	2015
8.	ITVL08	Aging-Aware Reliable Multiplier Design With Adaptive Hold Logic	POSITIVE BIAS TEMPERATURE INSTABILITY (PBTI)	2015
9.	ITVL09	Exact and Approximate Algorithms for the Filter Design Optimization Problem	FILTER DESIGN OPTIMIZATION PROBLEM	2015
10.	ITVL10	Ultralow-Energy Variation-Aware Design: Adder Architecture Study	STATISTICAL STATIC TIMING ANALYSIS (SSTA)	2015
11.	ITVL11	Fault Tolerant Parallel Filters	ERROR CORRECTION	2015

		Based on Error Correction Codes	CODES (ECCS)	
12.	ITVL12	Area-Delay-Power Efficient Carry-Select Adder	ARITHMETIC UNIT AND LOW-POWER DESIGN	2014
DOMAIN: HIGH SPEED				
13.	ITVL13	Variable Latency Speculative Han-Carlson Adder	MINECRAFT KOGGE STONE ADDER	2015
14.	ITVL14	A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications	HIGH-PERFORMANCE FIR FILTER	2015
15.	ITVL15	Fast Sign Detection Algorithm for the RNS Moduli Set $\{2^{n+1} - 1, 2^n - 1, 2^n\}$	RESTRICTED MODULI SET AND SIGN DETECTION	2015
16.	ITVL16	Energy-Efficient Approximate Multiplication for Digital Signal Processing and Classification Applications	ENERGY EFFICIENCY AND MULTIPLICATION	2015
17.	ITVL17	An Optimized Modified Booth Recoder for Efficient Design of the Add- Multiply Operator.	MODIFIED BOOTH RECODING	2014

18.	ITVL18	Low-Latency Successive-Cancellation Polar Decoder Architectures Using 2-Bit Decoding.	OVERLAPPED SCHEDULING, PRE COMPUTATION AND 2-BIT DECODER	2014
DOMAIN: QCA TECHNOLOGY				
19.	ITVL19	Coplanar Full Adder in Quantum-Dot Cellular Automata via Clock-Zone-Based Crossover	CARRY FLOW ADDER	2015
20.	ITVL20	Synthesis of Majority/Minority Logic Networks	MAJORITY GATES, QUANTUM-DOT CELLULAR AUTOMATA (QCA)	2015
21.	ITVL21	Design and simulation of Turbo encoder in quantum-dot cellular automata	TURBO ENCODER	2015
22.	ITVL22	Design of Efficient Binary Comparators in Quantum-Dot Cellular Automata.	MAJORITY GATES AND QUANTUM DOT CELLULAR AUTOMATA (QCA)	2014
23.	ITVL23	Area-Delay Efficient Binary	NANO COMPUTING	2014

		Adders in QCA.		
DOMAIN: DESIGN with TEST BENCH				
24.	ITVL24	Reverse Converter Design via Parallel-Prefix Adders: Novel Components, Methodology, and Implementations	RESIDUE NUMBER SYSTEM (RNS)	2015
25.	ITVL25	ERSFQ 8-Bit Parallel Adders as a Process Benchmark	ZERO STATIC POWER DISSIPATION	2015
26.	ITVL26	$(4 + 2\log n)\Delta G$ Parallel Prefix Modulo- $(2^n - 3)$ Adder via Double Representation of Residues in $[0, 2]$	DIGITAL SIGNAL PROCESSING	2015
DOMAIN:EDA TOOL (TANNER TOOL)				
27.	ITVL27	Energy and Area Efficient Three-Input XOR/XNORs With Systematic Cell Design Methodology	COMPLETELY SYMMETRIC HIGH MODULARITY LOGIC GATE	2015
28.	ITVL28	Single-Supply 3T Gain-Cell for Low-Voltage Low-Power Applications	ACCESS SPEED, DATA RETENTION TIME	2015

29.	ITVL29	Recursive Approach to the Design of a Parallel Self-Timed Adder	ASYNCHRONOUS CIRCUITS AND BINARY ADDERS	2015
30.	ITVL30	Low-Power Variation-Tolerant Nonvolatile Lookup Table Design	ROM DESIGN	2015
31.	ITVL31	Finite State Machines With Input Multiplexing: A Performance Study	ATM TRANSACTIONS	2015
32.	ITVL32	Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator	HIGH-SPEED ANALOG-TO-DIGITAL CONVERTERS (ADCS)	2014
33.	ITVL33	Universal Set of CMOS Gates for the Synthesis of Multiple Valued Logic Digital Circuits	MULTI VALUED LOGIC	2014
DOMAIN: VLSI with MATLAB				
34.	ITVL34	A Generalized Algorithm and Reconfigurable Architecture for Efficient and Scalable Orthogonal Approximation of	IMAGE COMPRESSION	2015

		DCT		
35.	ITVL35	Design and Analysis of Approximate Compressors for Multiplication	IMAGE MULTIPLICATION	2015
36.	ITVL36	An Analytical Framework for Evaluating the Error Characteristics of Approximate Adders	IMAGE PROCESSING	2015
37.	ITVL37	Efficient coding scheme for fault Tolerant parallel filter	CRYPTOGRAPHY	2015
38.	ITVL38	Input-Based Dynamic Reconfiguration of Approximate Arithmetic Units for Video Encoding	VIDEO DECODER	2015
39.	ITVL39	Improved 8-Point Approximate DCT for Image and Video Compression Requiring Only 14 Additions	HEVC	2014
40.	ITVL40	High-Throughput Multi		2014

		standard Transform Core Supporting MPEG /H.264/VC-1 Using Common Sharing Distributed Arithmetic	MULTI -STANDARD TRANSFORM (MST)	
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Education Partners:



Technologies and Domain used:

IEEE 2014, Java, J2ee, Android, Dot net, PHP, Embedded, Vlsi, Matlab, VB, Net working, Data Mining, Image Processing, Cloud Computing, Mobile Computing, Multimedia, Network Security, Soft Engg, Grid Computing, Automation, Robotics, Communication, RF, Zigbee, Blue tooth, GSM/GPS/GPRS, Power Electronics & Systems, Electrical, DSP, RTOS, Bio metrics, etc.

Features

- Latest 2014 IEEE, Science Direct, ACM based project concept and solutions.
- State of the art infrastructure, Innovative Project training methods.
- All our efforts are focused on students to meet industry requirements.
- Our environment is encapsulated with doctorates, professionals and other experts.
- Excellent Placements through our **Spiro HR Management Consultants (SMC) Pvt Ltd.**

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